DESIGNING OF A BRAIN STIMULATOR SUITABLE FOR INTRACRANIAL SELF-STIMULATION EXPERIMENTS FOR STUDYING THE BRAIN-STIMULATION REWARD SYSTEM

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(Received on March 20, 1985)

Summary : A circuit design has been developed and described for fabricating and using in the intracranial self-stimulation experiments on rat to study the brain-stimulation reward behaviour, and to explore into the underlying mechanisms of drives and motivated behaviours. The stimulator can be fabricated wiih parts available in India. It has been continuosly used and tested during the last four years in different research studies.

Key Words : brain-stimulator programmable pulse generator brain-stimulation reward

INTRODUCTION

For carrying on experiments in the field of intracranial self-stimulation as has been developed by Olds (vide Review of Olds, 1975), a pulse generator has been fabricated with components available in India. The pulse generator has been improved by using it during the last four years. The circuit of the stimulator and the principles of design are described in this paper. The design is independently developed and not a copy, hence is reported herein.

MATERIAL AND METHODS

The circuit diagram is provided in Fig. 1. A clock frequency is chosen at 1200 Hz, and is generated using a 555(IC_1) with suitable capacitor and adjustable preset potentiometer. The output, which is a squarewave of 50% duty cycle, is exactly set at 1200 Hz with the help of the preset potentiometer.

The 1200 cycles is simultaneouly divided by 7493(IC_2), a divided-by 16 counter, to give an output of 75 Hz and also by 7492 (IC_3), a divided by 12 counter, to give an

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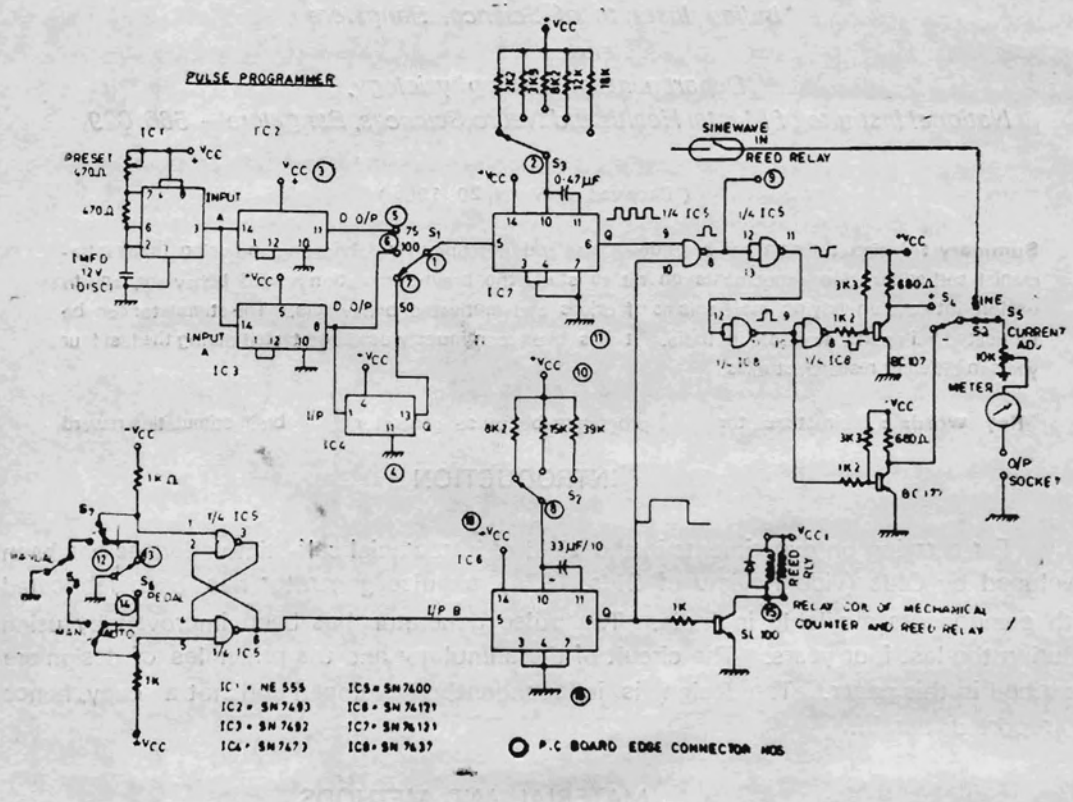
output of 100 Hz. The 100 Hz output is again divided by a 7473 (IC_4), a divided-by 2 counter, to obtain 50 Hz output. A panel mounted 1 pole 3 way switch S_1 will select any one of the above three frequencies for further processing.

Control of the pulse width is achieved by using a monostable multivibrator (IC_7) 74121. A panel mounted switch S_3 alters the various time constant resistors to give the 5 pulse widths needed, namely, 1/4, 1/2, 1, 2 and 4 milliseconds. The Q output of the 74121 is taken out.



Yet another 74121 (IC_6) controls the gate pulse width of 1/4, 1/2 and 1 sec. Switch S_2 switches the necessary time constant resistors for this duration.

The Q output of IC_6 is also selected to operate the gate formed by 1/4 of IC_5. When the output is present at pin 10 of IC_5, it opens the gate and allows the pulse train from IC_7 till the preset time is over. Then Q output of IC_6 will cease to exist. However, it should be noted that the selected frequency squarewave with suitable pulse width is always present at pin 9 of IC_5 and is allowed as and when required by opening the gate with IC_6.

IC_6 is started with a single pulse whose duration is determined by the timing component selected by the switch S_2. The single pulse has to be provided either manually or with the pedal incorporated in the cage. S_7, a single pole double throw switch does this. To avoid multi switching, $\frac{1}{2}$ of IC_5 is used as the bounce-proof switch to give always a single pulse each time S_6 is activated.

It is also needed to count the number of times switch S_6 is pressed. The Q output of IC_6 is taken out to a drive transistor SL100 and each time S_6 is activated, the +Ve pulse at Q will drive the transistor to saturation. The electro-mechanical resettable counter connected in the Collector Circuit will register a count. Diode connected across the counter prevents the back EMF generated by the coil, from destroying the transistor. The same output will drive a reed relay to allow the sine wave to be available at switch S_5.

The output of IC_5 at pin 8 is not capable of driving the necessary current. Hence, it is buffered with 2 gates, so that the final output is a replica of the original.

The +ve going pulse at pin 11 of IC_8 is used to drive a PNP transistor BC 177, already kept under saturation condition, so that the output at its collector is zero i.e. at ground potential. As soon as a +ve pulse arrives at the base, it counteracts the –ve bias and the transistor goes into cut-off, and the full voltage appears at the collector till the pulse lasts, thus giving a –ve pulse.

Similarly, an NPN transistor BC107 is kept at saturation with a bias resistor. On arrival of a –ve pulse at the base, it snaps into non-conduction, thus giving a +ve pulse at the Collector.

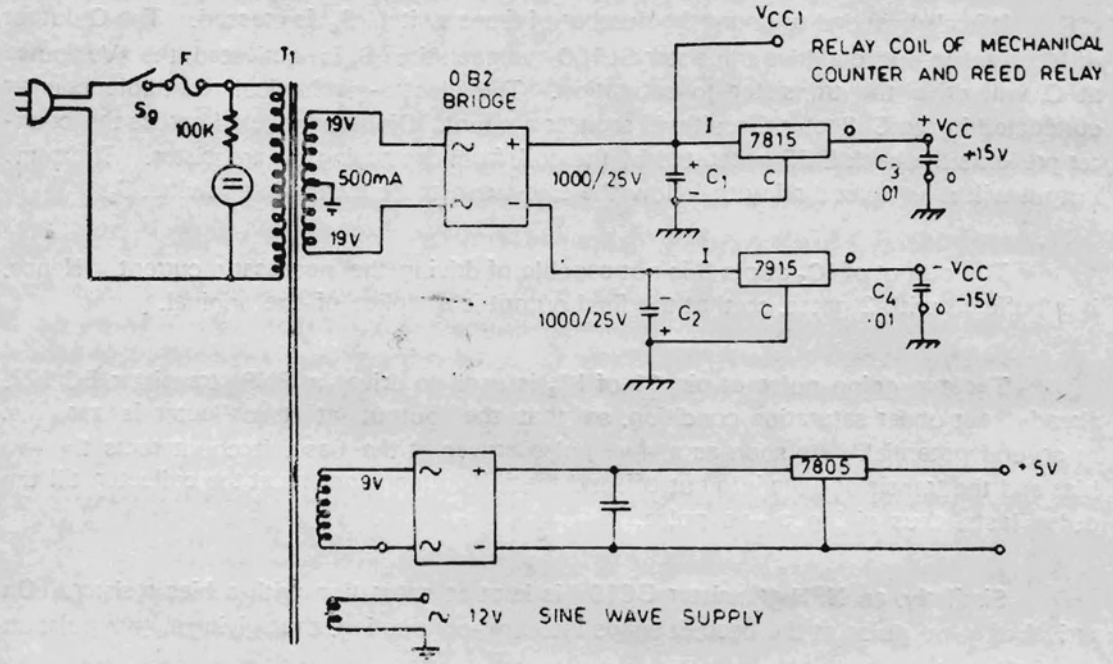
A switch S_4 selects either one of those pulses and is taken out. Variable resistance 10 K will control the current flowing through the load and a micro-amp meter will read the average current flowing through it.

S_5 will select either the sine wave that is available for .25, .5, or 1 sec. and passes through the current setting potentiometer. As the sine wave is obtained directly from the transformer it is capable of driving the necessary current.

Power supply : The unit needs a stabilized supply of +5 volts for the operation of the digital integrated circuit. This is derived from the rectified output +ve voltage and is stabilized with a 3-terminal regulator 7805. The +ve and –ve pulses need $\pm$ 15 volts supply respectively. These are rectified and stabilized from a 19-0-19 transformer and stabilized with a 7815 and 7915 three-terminal regulators (Fig. 2).

The electrolytic capacitors C_1, C_2 filter the DC supply, and the C_3, C_4 will protect the circuit from transients.

Finally the mechanical counter needs a supply of 12 to 15V unregulated DC, and is derived from the +ve unregulated supply.



RESULTS

The stimulator can deliver pulses for a fixed duration preset by the gate switch. During the open gate condition, the train of pulses is delivered into the brain tissue. The gate openings can be repeated up to 4 times a second. The electro-mechanical counter indicates the number of times the gate switch is operated.

The stimulator will provide the following specifications :—

1. Square wave pulse frequency selectable in 3 steps 50-75-100Hz or since wave at 50 Hz.
2. Square pulse polarity reversable with reference to the ground.
3. Square pulse width switchable to set at 1/4, 1/2, 1, 2 and 4 msec.

4. Gate opening timings switchable to set at 250, 500, 1000 msec.
5. Pulse height 15 volts and capable of driving upto 3 mA into 5K external load resistance.
6. Triggering – Mannually or with a pedal microswitch.
7. Gate count with an electro-mechanical counter.

The gate switch of the pulse generator can be linked to a pedal for the operation by the experimental subject (e.g. rat). If the rat presses on the pedal, the gate switch opens and the output of the stimulator is delivered via electrodes implanted in the brain of the rat and connected to the output of the stimulator. This type of experimentation is used to survey the brain substrates of "pleasure" or rewards and drive and motivation.

ACKNOWLEDGEMENTS

The support of the Indian Council of Medical Research is acknowledged.

REFERENCE

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